Organic Thin-Film Transistors with Anodized Gate Dielectric Patterned by Self-Aligned Embossing on Flexible Substrates

Yiheng Qin, Daniël H. Turkenburg, Ionut Barbu, Wiljan T. T. Smaal, Kris Myny, Wan-Yu Lin, Gerwin H. Gelinck, Paul Heremans, Johan Liu, and Erwin R. Meinders*

An upscalable, self-aligned patterning technique for manufacturing high-performance, flexible organic thin-film transistors is presented. The structures are self-aligned using a single-step, multi-level hot embossing process. In combination with defect-free anodized aluminum oxide as a gate dielectric, transistors on foil with channel lengths down to 5 μm are realized with high reproducibility. Resulting on-off ratios of 4×10^6 and mobilities as high as 0.5 $cm^2\ V^{-1}\ s^{-1}$ are achieved, indicating a stable process with potential to large-area production with even much smaller structures.

1. Introduction

Thin-film transistors (TFTs), either with organic or inorganic semiconductor materials, have been proposed for various applications in large-area electronics on flexible substrates, for instance, active-matrix displays,[1–3] radio-frequency identification (RFID) tags,[4] and sensor arrays.[5,6] Several challenges remain in the realization of high-performance TFTs on flexible polymeric substrates. To improve the drive current capacity of organic TFTs (OTFTs), generally characterized by low charge carrier mobilities (below 10 $cm^2\ V^{-1}\ s^{-1}$), basic device physics commands to use small transistor channel lengths, which is challenging because of the need to form these reproducibly and with perfect alignment between the gate and the source/drain on dimensionally unstable plastic foils, and gate dielectrics with a high dielectric constant (high *k*), which need to be applicable on plastic substrates at low temperature. Regarding the latter, anodized aluminum (Al)[7,8] has been shown to be a promising dense, uniform, and high-*k* dielectric layer at low temperature, with good adhesion to the underlying metal and applicable with cost-effective equipment. The current solution to increase the dimensional stability of flexible substrates is to temporary bond them on a rigid carrier, called the foil-on-carrier (FOC) approach.[9] A further improvement to overcome alignment errors on instable substrates is to use self-aligned patterning, such as self-aligned imprint lithography (SAIL)[10–12] or self-aligned printing[13,14] in which a multi-layer stack of functional layers is patterned in one single imprint step using a multi-level imprint stamp. For a TFT, the source/drain, gate, and gate dielectric geometries are casted in a multi-level stamp and transferred to the substrates via selective etching of a metal-insulator-metal (MIM) stack prepared on the foil. The potential of patterning ultrafine features[15] makes this technology very attractive for TFT applications. In this study, we present a technology for self-aligned bottom-gate, bottom-contact organic TFTs (OTFTs) on flexible substrates having anodized aluminum oxide (Al_2O_3) gate dielectric. The patterning process is realized by one-step, multi-level hot embossing (thermal imprinting) on a large-area, defect-free MIM stack instead of patterning the structures layer by layer with alignment. Such self-aligned embossing process starting from an uniform non-patterned stack allows the use anodized aluminum oxide as a dielectric since the non-patterned gate metal can function as the counter electrode in the anodization process. We demonstrate OTFT channel lengths down to 5 μm and a good electrical performance with high reproducibility. The results are promising in view of large-area production, potentially involving even much smaller structures.

Y. Qin, D. H. Turkenburg, I. Barbu, W. T. T. Smaal, Dr. G. H. Gelinck, Dr. E. R. Meinders
Holst Centre
TNO-The Dutch Organization for Applied Scientific Research
High Tech Campus 31, 5656 AE Eindhoven, the Netherlands
E-mail: daniel.turkenburg@tno.nl
K. Myny, W.-Y. Lin, Prof. P. Heremans
Imec, Kapeldreef 75, B-3001 Leuven, Belgium
Y. Qin, Prof. J. Liu
Department of Microtechnology and
Chalmers University of Technology
Kemivägen 9, SE 412 96 Göteborg, Sweden

DOI: 10.1002/adfm.201102266

2. Fabrication Processes of Self-Aligned OTFTs

Figure 1 is the schematic illustration of the self-aligned embossing patterning process that we developed for manufacturing bottom-gate, bottom-contact TFTs. Polyethylene naphthalate (PEN) foil is temporarily bonded to a rigid substrate via a roller laminator. SU-8 photoresist is spin-coated on top of the foil to reduce the surface roughness of polymeric substrate. Subsequently, the MIM stack is deposited onto the prepared FOC substrate. Taking into account the thermal stability of the PEN foil, the gate layer is deposited by sputtering 150 nm Al at

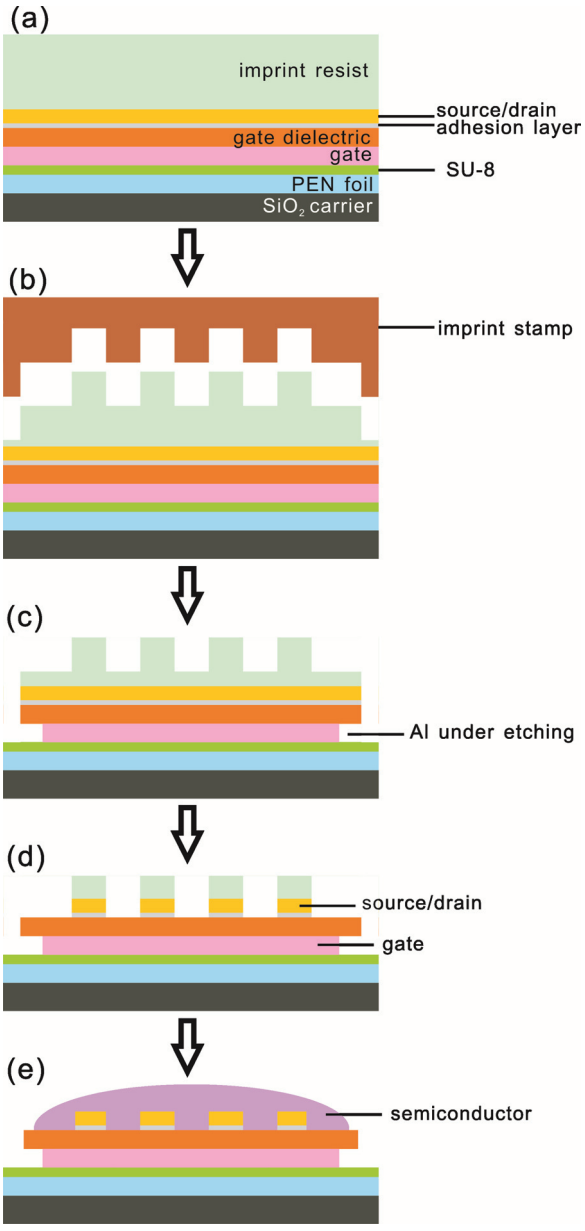

Figure 1. Process flow of an OTFT fabricated by self-aligned embossing. a) Definition of the MIM stack and imprint resist. b) 3D geometry formation in the resist layer by hot embossing. c) First MIM stack patterning (gate patterning). d) Second MIM stack patterning (source/drain patterning, source/drain self-aligned to gate/dielectric). e) Removal of residual resist and semiconductor inkjet printing.

low power in order to keep it at room temperature. Then the anodization is carried out in an experimental set up, according to Equation 1:

$$2Al + 3H_2O \rightarrow Al_2O_3 + 3H_2 \uparrow \quad (1)$$

In order to obtain 60 nm thick dense, uniform, barrier-type anodized Al_2O_3 layer as the gate dielectric, a solution with tartaric acid and ethylene glycol is prepared as the anodization electrolyte with the anodization voltage of 40 V. Subsequently, the source/drain layer is formed by sputtering 5 nm chromium (Cr) and 50 nm gold (Au) onto the anodized Al_2O_3 at low power. Hot embossing, rather than UV imprinting, is chosen as the patterning method, allowing wider range selections of materials. To that end, a layer of 335 nm mr-I7030R thermal imprint resist (purchased from Micro-resist Technology GmbH) is spin-coated onto the MIM stack (Figure 1a). Figure 1b describes the embossing process: a multi-level stamp with embedded TFT structures of various channel width (W)/channel length (L) is prepared. Before embossing, the surface of the Ni stamp is treated with a monolayer of 1H,1H,2H,2H-perfluorooctyltrichlorosilane (PFDTS) to improve the releasing property of the stamp.[16] The stamp is then pressed into the resist layer on the MIM stack with a typical pressure of 4×10^6 Pa while the substrate is heated up to 160 °C. The embossing process lasts for 5 min and then both the stamp and the substrate are cooled down to 50 °C before the stamp is released from the substrate. Therefore, 3D structures are defined in the resist layer (Figure 1b). When the residual layer of the imprinted resist layer is anisotropically removed by O_2 plasma reactive ion etching (RIE), the pattern is transferred to the MIM stack layer-by-layer via a selective wet etching process using the residual resist as the etching mask. Among these steps, the Al and anodized Al_2O_3 layers are simultaneously etched in an acid etchant that has a faster etch rate towards Al than towards Al_2O_3. This simultaneous etching leads to an under-etching of the Al layer, which allows proper isolation between gate and source/drain (Figure 1c). Figure 1d illustrates the second step of MIM stack patterning where RIE and wet etching are still the routes to pattern the source and drain electrodes. So far, the three-layer MIM structure has been patterned via one single embossing process with all the layers intrinsically aligned with respect to each other. Finally, the residual imprint resist is removed and self-assembled monolayers (SAMs) of pentafluorobenzenethiol (PFBT) as well as trichlorophenylsilane (TCPS) are deposited. Blends of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) and polystyrene are prepared in tetraline solution as the semiconductor ink and inkjet-printed to the top of TFTs when the substrate is heated up to 70 °C (Figure 1e).[17–20]

3. Results and Discussion

3.1. Metal-Insulator-Metal Stack Deposition

The self-aligned embossing based patterning technique requires the deposition of MIM stack before the patterning. This is compatible with the use of anodization to form a blanket layer of Al_2O_3 starting from a blanket layer of Al. According to previous results,[21] a high dielectric surface roughness would lower the carrier mobility in the organic semiconductor, hence affecting the OTFT's performance. That is why a planarization layer is used on the FOC system. However, in such process described above, we observed that the stress created by the volume expansion of Al during anodization[22] is prone to give rise to bubble-shape defects as shown in **Figure 2**a. They may be caused by poor adhesion between metal and the planarization layer applied on the PEN foil substrate as well as by initial defects (pin-holes, particles, etc.) in the as-deposited metal layer. An

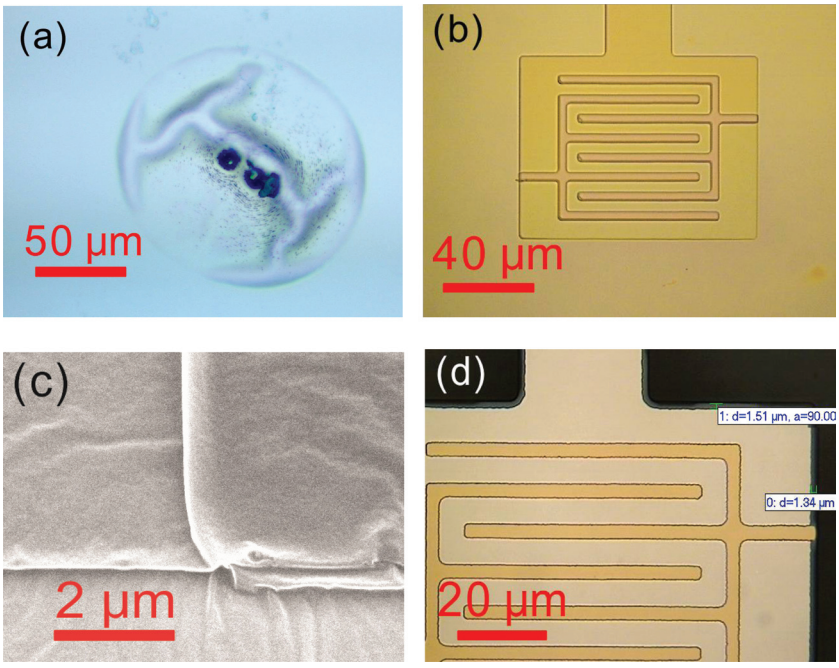

Figure 2. a) Microscopy image of one of the defects generated in the Al anodization process. b) Microscopy image of the resist morphology on the MIM stack defining the TFT structures after imprinting. c) SEM image illustrating the clearly defined three-level resist morphology after embossing. d) Microscope image of the patterned TFT structure with 1.5 µm Al under etching on the structure edge.

optimized adhesion layer and process is described in **Table 1**, which gives an overview of measures that allow reducing or even eliminating delamination defects. On the one hand, it is obvious that a planarization layer is able to reduce the dielectric surface roughness by around 64% (root-mean-square (RMS) value from 11 nm down to 4 nm measured by atom force microscopy (AFM), **Figure 3**) when the Al thickness of 150 nm is unchanged. On the other hand, improved adhesion[23] by using SU-8 3005 photoresist instead of SU-8 2002 as planarization layer, including out gassing and soft etching steps before Al sputtering could prevent the generation of defects. This process is selected as the optimized one for our further manufacturing. It could also be observed that depositing thicker Al helps to eliminate defects, but results in rougher surfaces. Comparing to the solution of adding in a barrier layer between the polymer substrates and metal layer reported elsewhere,[24] our approach is easier in processing and could avoid potential problems by bringing in one additional layer. Using this optimized process, a flat, defect-free and uniform dielectric layer with 0.5 nm thickness variation over 100 mm wafer area is obtained. See Figure S1 in the Supporting Information for more details.

3.2. Self-Aligned Embossing

The full MIM stack with embossed resist polymer is shown in Figure 2b (schematic illustration in Figure 1b). The gate and source/drain structures are clearly defined in the resist layers with a feature size of 5 µm on this example and the resist morphology is inspected by scanning electron microscopy (SEM), shown in Figure 2c. The height difference between different embossed resist layers is around 250 nm, indicating there is no filling issue regarding the flow of resist in the stamp. The TFT structures are then successfully transferred to the MIM stack by selective etching and no cross-etching or delamination phenomenon is observed (Figure 2d), leading to the well-aligned source/drain fingers above the gate area. Since the wet etching process is crucial towards the MIM stack, which is exposed to various etchants in multiple cycles, our result shows a chemically and mechanically reliable MIM stack. We thus demonstrate the self-alignment of gate/dielectric and source/drain patterns using a single rigid multi-level imprint step without employing alignment marks, ensuring the relative position between gate and

Table 1. Overview of the quality of the dielectric manufactured by different process steps.

Substrate	Planarization layer	Thickness of Al [nm]	Out gassing of SU-8	Sputter etching on SU-8	Amount of defects	Dielectric surface roughness[a] [nm]
SiO_2	SU-8 2002	150	–	–	No	5
SiO_2	SU-8 2002	150	–	–	Some	–
FOC	–	150	–	–	No	11
FOC	SU-8 2002	150	–	–	Many	5
FOC	SU-8 3005	150	–	–	Some	–
FOC	SU-8 3005	150	Yes	–	Some[b]	–
FOC	SU-8 3005	150	Yes	Yes	No	4
FOC	SU-8 3005	400	Yes	-	No	8
FOC	SU-8 3005	400	Yes	Yes	No	8

[a] RMS value; [b] Less defects than the sample of FOC with SU-8 3005 planarization layer but without out gassing step.

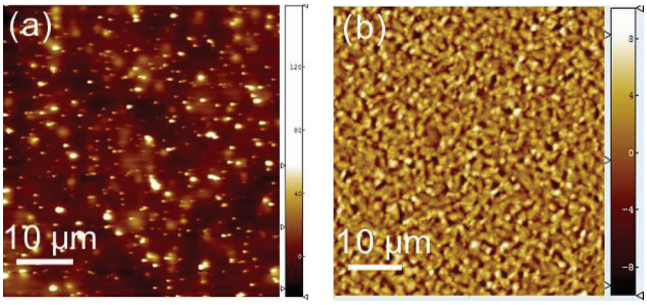

Figure 3. Dielectric surface roughness. a) Sample without planarization layer. b) Sample with SU-8 3005 planarization layer. Unit in the color scale bar: nm.

source/drain can hardly change despite the substrate waviness and further processing steps. Moreover, there is about 1.5 µm under etching distance in the Al layer underneath the Al_2O_3 is achieved in Figure 2d. Some line edge roughness of the over etched Al can be observed, but it is insignificant comparing to the channel length, which allows us to apply this technique with smaller features in the future.

3.3. Devices Characterization

To finalize the TFT testing structure (Figure 1e, **Figure 4**a), vias are etched in the Al_2O_3 layer by boron trichloride RIE in the contact pads area. Connections between devices and contact pads are deposited and patterned by lift-off process of 5 nm thick Ti and 100 nm thick Au. Only coarse alignment is required for these interconnect lines. Finally, the organic semiconductor material, blends of TIPS pentacene and polystyrene, is inkjet printed on top of the structure, whereby care is taken that the surface wetted by the drops is in good agreement with the gate size to prevent the overflowing of semiconductor to the substrate, which would result in a leakage path between source/drain and gate.

The electrical characterization of the OTFTs is performed in an argon atmosphere. The voltage between source and drain is set to –1 V for the linear region and to –10 V for the saturation region, followed by sweeping the gate voltage from +10 V to –10 V in bi-direction scan mode. The transfer and output characteristic curves of four OTFTs (W = 1000 µm, L = 5 µm) are shown in Figure 4b,c. The close-to-zero switch-on voltage and steep sub-threshold slope are obtained. The average carrier mobilities when the OTFT works in the saturation and linear region are 0.5 $cm^2\ V^{-1}\ s^{-1}$ and 0.4 $cm^2\ V^{-1}\ s^{-1}$, respectively, which agree well with recent results on TIPS pentacene-based transistors.[17,25,26] In addition, an average on/off ratio of 4×10^6 is obtained and the gate current is kept at the level of 10 pA, both of which demonstrate the promising quality of the anodized gate dielectric. On the same sample, there are also OTFTs with channel lengths of 10 µm and 20 µm, whose electrical performance and yield rate are shown in **Table 2** as well as in the supporting information.

As shown in Table 2, the yield is lower for OTFTs with shorter channel length. The main yield-limiting factor is electrical shorts related to imperfections in the multilevel imprint stamp.

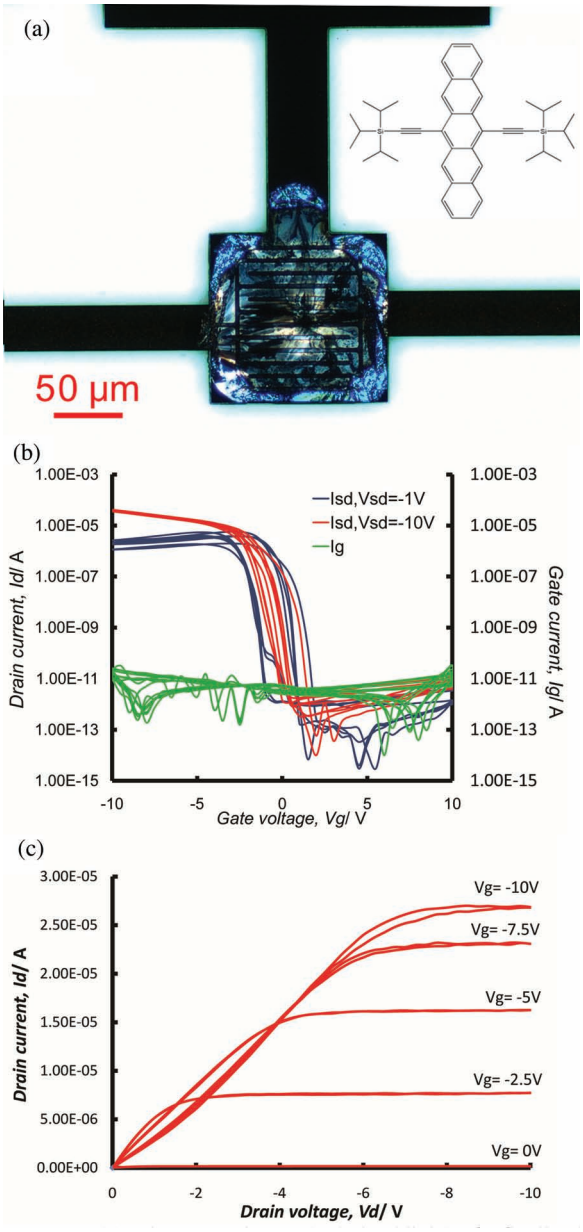

Figure 4. a) Microscopy image (polarized light) of a finalized OTFT (W = 1000 µm, L = 5 µm) with inkjet-printed TIPS pentacene. b) Transfer characteristic curves of four OTFTs (W = 1000 µm, L = 5 µm). Output characteristic curves of a OTFT (W = 1000 µm, L = 5 µm).

In Figure 4b as well as Figure S2b,d, some hysteresis is observed in the transfer characteristics, which we attribute to hydroxyl impurities that are formed in the anodized dielectric layer,[8] in agreement with earlier observations.[8,27–29] Hysteresis could be improved by a post-baking step in vacuum directly after Al anodization.[30]

The device characteristics show certain non-idealities, such as a contact resistance that is clearly visible in the linear regime. Hydroxyl groups at the dielectric surface might also be one of the reasons to the non-ideal curve and affect the contact between source/drain electrode and semiconductor. Besides,

Table 2. Electrical performance and yield rate of OTFTs with various channel lengths.

Channel length [μm]	Linear mobility [$cm^2 V^{-1} s^{-1}$]	Saturation mobility [$cm^2 V^{-1} s^{-1}$]	On/off ratio	Yield rate
5	0.40 ± 0.12	0.50 ± 0.10	$4.0 \times 10^6 \pm 2.1 \times 10^6$	20% (4 out of 20)
10	0.43 ± 0.10	0.54 ± 0.09	$3.0 \times 10^6 \pm 1.6 \times 10^6$	60% (132 out of 220)
20	0.49 ± 0.08	0.60 ± 0.08	$1.2 \times 10^6 \pm 4.0 \times 10^5$	100% (220 out of 220)

the 5 nm Cr adhesion layer is close to the dielectric surface contacting the channel, which would also contribute to a high contact resistance.

4. Conclusions

In summary, we have developed a self-aligned embossing patterning technique to manufacture bottom-gate, bottom-contact organic TFTs. The MIM stack with defect-free, flat, and uniform anodized Al_2O_3 dielectric layer is deposited on flexible PEN foil substrate. A multi-level imprint stamp is prepared to define the 3D structure in the imprint resist by hot embossing. The self-aligned OTFT structures with 5 μm feature size are then demonstrated via layer-by-layer selective etching of the MIM stack without using alignment between layers. To finalize the devices, TIPS pentacene is deposited on top of each TFT structure by inkjet printing. Electrical measurements show promising carrier mobility and on/off ratio. The high reproducibility also indicates the potential of introducing this technique into large area production. Our approach is different from other self-aligned approaches,[12–14] which put a strong focus on a maximal reduction of parasitic overlap capacitance between the source/drain and gate for high-frequency TFT applications. We prefer to emphasize the compatibility of our method with the use of anodized Al_2O_3 combined with organic semiconductor of blends of TIPS pentacene and polystyrene, which accounts for the obtained on-current of the OTFTs that is at least 100 times higher than other self-aligned TFTs.[11–14,31] Moreover, anodized Al_2O_3 is preferred because of its high breakdown strength compared to the polymer dielectric, which makes it is easier reduce parasitic overlap capacitance.[7,12] With our process and materials we also report a high yield rate (100% for 20 μm structures), which is not mentioned by the other approaches.

For further development, TFTs with sub-micrometer or even smaller channel lengths are to be manufactured using this technique. Parasitic overlap capacitance could be reduced by fine tuning the under etching of Al or by making smaller source/drain fingers in other forms of circuit layout to improve high-frequency performance of the TFTs. Our self-aligned embossing patterning technique can be scaled up to fabricate complementary circuits by employing n-type semiconductors such as indium-gallium-zinc oxide (IGZO).[7,32,33] Via filling and connection, wires could also be imprinted by adding corresponding structures into the stamp using material subtractive[10] or additive[34,35] approaches with the potential for integrating the steps of material deposition, imprinting, and etching into a roll-to-roll process line.[10,34,36]

5. Experimental Section

FOC and Planarization Layer Preparation: A silcon wafer was cleaned by O_2 plasma at 90 °C for 5 min, then 500 nm thick oxide was thermally grown on both sides and behaves as the carrier. A 25 μm thick PEN foil with temporary adhesive on one side (Q83 type, supplied by DuPont Teijin Films) was laminated on to the polished side of the wafer by a roller laminator with a pressure of 3×10^5 Pa at 90 °C. The adhesive between the foil and carrier was activated by heating to 170 °C in an oven for 1 h and was then cooled under ambient conditions. An SU-8 3005 (purchased from MicroChem Corp.) photoresist layer was spin-coated on the laminated PEN foil and acted as the planarization layer. The out gassing was carried out at 130 °C for 12 h under vacuum.

MIM Stack Fabrication: A Veeco 2 Nexus sputter tool was used to sputter-etch the SU-8 planarization for 30 s. The sputtering of the 150 nm Al as gate layer was carried out using the same equipment with a deposition rate of 1.74 nm s^{-1}. The anodization electrolyte was a solution of tartaric acid (0.07 mol dm^{-3}) in a 1:2 (V:V) mixture of water and ethylene glycol, which was brought to pH 6.3 with an aqueous solution of ammonia (1% w/w). The anodization was carried out by setting a constant current density of 0.3 mA cm^{-2} before the voltage was increased to 40 V during 15 min, leading to a 60 nm thick Al_2O_3 gate dielectric layer. Veeco CVC Connexion 800 sputter tool was used to deposit 5 nm Cr and 50 nm Au as the source/drain layers with the deposition rates of 0.37 nm s^{-1} and 0.32 nm s^{-1}, respectively.

Resist and MIM Stack Etching: The imprint resist was anisotropically etched in a STS Multiplex clustertool by an O_2 plasma with the etching rate of 1.30 nm s^{-1}. Au was wet-etched in an aqueous solution of potassium iodide (0.30 mol dm^{-3}) and iodine (0.05 mol dm^{-3}), with an etching rate of 3.92 nm s^{-1} at 21 °C. Cr was wet-etched in an aqueous solution of perchloric acid (0.50 mol dm^{-3}) and ceric ammonium nitrate ($(NH_4)_2[Ce(NO_3)_6]$, 0.23 mol dm^{-3}) with the etch rate of 1 nm s^{-1} at 21 °C. Al and anodized Al_2O_3 were simultaneously etched in a commercial H_3PO_4/HNO_3 etchant (PS 70-10 VLSI Selectipur, supplied by BASF), with the etching rates of 10 nm s^{-1} and 2 nm s^{-1}, respectively.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was financially supported by the European-funded project ORICLA (FP7-ICT No. 247798). J.L. acknowledges the financial support from Chalmers Strategic Initiative in Production.

Received: September 22, 2011
Revised: November 18, 2011
Published online: January 18, 2012

[1] M. L. Chabinyc, A. Salleo, *Chem. Mater.* **2004**, *16*, 4509.
[2] G. H. Gelinck, H. E. A. Huitema, E. Van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. Van Der Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B. H. Huisman, *Nat. Mater.* **2004**, *3*, 106.
[3] C. Sheraw, L. Zhou, J. Huang, D. Gundlach, T. Jackson, M. Kane, I. Hill, M. Hammond, J. Campi, B. Greening, *Appl. Phys. Lett.* **2002**, *80*, 1088.

[4] K. Myny, S. Steudel, P. Vicca, M. J. Beenhakkers, N. A. J. M. van Aerle, G. H. Gelinck, J. Genoe, W. Dehaene, P. Heremans, *Solid-State Electron.* **2009**, *53*, 1220.
[5] L. Wang, D. Fine, A. Dodabalapur, *Appl. Phys. Lett.* **2004**, *85*, 6386.
[6] Z. T. Zhu, J. T. Mason, R. Dieckmann, G. G. Malliaras, *Appl. Phys. Lett.* **2002**, *81*, 4643.
[7] W.-Y. Lin, R. Müller, K. Myny, S. Steudel, J. Genoe, P. Heremans, *Org. Electron.* **2011**, *12*, 955.
[8] L. Majewski, M. Grell, S. Ogier, J. Veres, *Org. Electron.* **2003**, *4*, 27.
[9] M. van Neer, D. van den Berga, P. Giesen, K. Tempelaars, S. Green, M. van de Moosdijk, E. R. Meinders, I. Yakimets, Fabrication of flexible display backplanes on high temperature resistant polymer substrates, presented at *Int. Conf. on Organic Electronics, Roma*, June 2011.
[10] H. J. Kim, M. Almanza-Workman, B. Garcia, O. Kwon, F. Jeffrey, S. Braymen, J. Hauschildt, K. Junge, D. Larson, D. Stieler, A. Chaiken, B. Cobene, R. Elder, W. Jackson, M. Jam, A. Jeans, H. Luo, P. Mei, C. Perlov, C. Taussig, *J. Soc. Inf. Display* **2009**, *17*, 963.
[11] E. Lausecker, Y. Huang, T. Fromherz, J. C. Sturm, S. Wagner, *Appl. Phys. Lett.* **2010**, *96*, 263501.
[12] U. Palfinger, C. Auner, H. Gold, A. Haase, J. Kraxner, T. Haber, M. Sezen, W. Grogger, G. Domann, G. Jakopic, *Adv. Mater.* **2010**, *22*, 5115.
[13] S. Li, W. Chen, D. Chu, S. Roy, *Adv. Mater.* **2011**, *23*, 4107.
[14] K. D. Kim, T. M. Lee, J. D. Jo, B. O. Choi, D. S. Kim, *J. Korean Phys. Soc.* **2009**, *54*, 489.
[15] M. D. Austin, H. Ge, W. Wu, M. Li, Z. Yu, D. Wasserman, S. Lyon, S. Y. Chou, *Appl. Phys. Lett.* **2004**, *84*, 5299.
[16] M. Beck, M. Graczyk, I. Maximov, E. L. Sarwe, T. Ling, M. Keil, L. Montelius, *Microelectron. Eng.* **2002**, *61*, 441.
[17] X. Li, W. T. T. Smaal, C. Kjellander, B. van der Putten, K. Gualandris, E. C. P. Smits, J. Anthony, D. J. Broer, P. W. M. Blom, J. Genoe, *Org. Electron.* **2011**, *12*, 1319.
[18] J. E. Anthony, J. S. Brooks, D. L. Eaton, S. R. Parkin, *J. Am. Chem. Soc.* **2001**, *123*, 9482.
[19] S. R. Saudari, Y. J. Lin, Y. Lai, C. R. Kagan, *Adv. Mater.* **2010**, *22*, 5063.
[20] M. Mas-Torrent, C. Rovira, *Chem. Rev.* **2011**, *111*, 4833.
[21] S. Steudel, S. De Vusser, S. De Jonge, D. Janssen, S. Verlaak, J. Genoe, P. Heremans, *Appl. Phys. Lett.* **2004**, *85*, 4400.
[22] O. Jessensky, F. Muller, U. Gosele, *Appl. Phys. Lett.* **1998**, *72*, 1173.
[23] Product information from MicroChem Corp., http://www.microchem.com/pdf/SU-8-table-of-properties.pdf (accessed May 2011).
[24] M. J. Lee, K. S. Chung, J. I. Han, S. K. Park, S. J. Hong, D. S. Kim, *J. Korean Phys. Soc.* **2002**, *41*, 795.
[25] J. H. Bae, H. Kim, G. Horowitz, S. D. Lee, *Solid-State Electron.* **2011**, *63*, 163.
[26] D. Hwang, C. Fuentes-Hernandez, J. Kim, W. Potscavage Jr., B. Kippelen, *Org. Electron.* **2011**, *12*, 1108.
[27] R. Street, A. Salleo, M. Chabinyc, *Phys. Rev. B* **2003**, *68*, 085316.
[28] I. Torres, D. Taylor, E. Itoh, *Appl. Phys. Lett.* **2004**, *85*, 314.
[29] S. Goettling, J. Brill, N. Fruehauf, J. Pflaum, E. Margallo-Balbás, *Proc. SPIE* **2005**, *5940*, 594010.
[30] R. B. Heimann, *Classic and advanced ceramics: from fundamentals to applications*, Wiley-VCH, Weinheim, Germany **2010**, Ch. 7.
[31] A. Jeans, M. Almanza-Workman, R. Cobene, R. Elder, R. Garcia, F. Gomez-Pancorbo, W. Jackson, M. Jam, H. J. Kim, O. Kwon, F. Jeffrey, S. Braymen, J. Hauschildt, K. Junge, D. Larson, D. Stieler, *Proc. SPIE* **2010**, *7637*, 763719.
[32] J. Park, I. Song, S. Kim, C. Kim, J. Lee, H. Lee, E. Lee, H. Yin, K. K. Kim, *Appl. Phys. Lett.* **2008**, *93*, 053501.
[33] J. K. Jeong, J. H. Jeong, H. W. Yang, J. S. Park, Y. G. Mo, H. D. Kim, *Appl. Phys. Lett.* **2007**, *91*, 113505.
[34] P. Maury, D. Turkenburg, N. Stroeks, P. Giesen, I. Barbu, E. Meinders, A. van Bremen, N. Iosad, R. van der Werf, H. Onvlee, *Microelectron. Eng.* **2011**, *88*, 2052.
[35] C. E. Hendriks, P. J. Smith, J. Perelaer, A. M. J. van den Berg, U. S. Schubert, *Adv. Funct. Mater.* **2008**, *18*, 1031.
[36] C. Yang, K. Shin, S. Y. Yang, H. Jeon, D. Choi, D. S. Chung, C. E. Park, *Appl. Phys. Lett.* **2006**, *89*, 153508.